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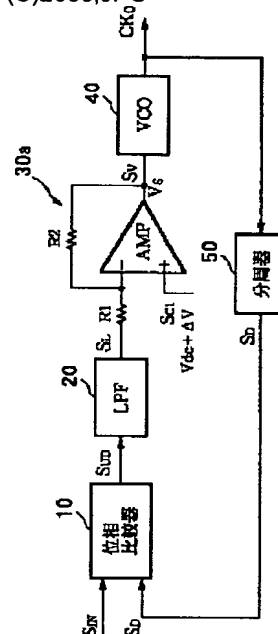
(21) Application number: **10265457**(71) Applicant: **SONY CORP**(22) Date of filing: **18.09.98**(72) Inventor: **SONEDA MITSUO**(54) **CLOCK GENERATING CIRCUIT**

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## (57) Abstract:

**PROBLEM TO BE SOLVED:** To realize a clock-generating circuit that realizes spread spectrum processing for a clock signal and reduces the radiation of electromagnetic waves by shifting only slightly an operating clock signal of a semiconductor device.

**SOLUTION:** A phase comparator 10 of a PLL circuit compares a phase of a received reference clock signal SIN with a phase of a frequency division signal SD from a frequency divider 50, outputs an up-down signal SUD in response to a phase difference of the signals, a low-pass filter 20 eliminates a high frequency component of the up-down signal SUD and provides an output of a signal SL, consisting of low frequency components. A DC amplifier 30a generates a control signal SV resulting from adding a bias signal, in response to a frequency control signal SC1 to the signal SL and gives the signal SV to a VCO 40, the VCO 40 oscillates at a frequency set by the control signal SV and generates a clock signal CK0, whose frequency is transited in response to the frequency control signal SC1 and gives it to a semiconductor device as an operating clock signal.



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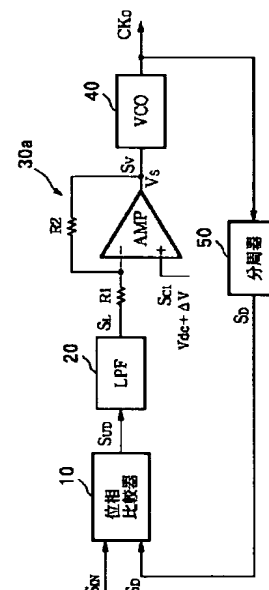
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(54) 【発明の名称】 クロック発生回路

(57) 【要約】

【課題】 半導体装置の動作クロック信号をわずかに遷移させることにより、クロック信号のスペクトラム拡散を実現でき、電磁波輻射を低減できるクロック発生回路を実現する。

【解決手段】 PLL回路において位相比較器 10 は入力した基準クロック信号  $S_{IN}$  と分周器 50 からの分周信号  $S_D$  との位相を比較し、これらの信号の位相差に応じてアップダウン信号  $S_{UD}$  を出力し、ローパスフィルタ 20 はその高周波成分を除去し、低周波成分からなる信号  $S_L$  を出力する。直流増幅器 30a は信号  $S_L$  に周波数制御信号  $S_{C1}$  に応じたバイアス信号を加えた制御信号  $S_V$  を生成し、VCO 40 に供給し、VCO 40 は制御信号  $S_V$  により設定した周波数で発振し、周波数制御信号  $S_{C1}$  に応じて周波数が遷移するクロック信号  $CK_0$  を発生し、動作クロック信号として半導体装置に供給する。



## 【特許請求の範囲】

【請求項1】 入力されたクロック信号を積分し、当該クロック信号の立ち上がりおよび立ち下がりにおける時間に対するレベル変化の傾きを緩やかにした積分クロック信号を出力する積分回路と、

上記入力クロック信号より低い周波数でレベルを変化する周波数制御信号に応じて上記積分クロック信号をレベル制限し、周波数が上記周波数制御信号に従って変化する第2のクロック信号を出力するリミッタ回路と、  
上記第2のクロック信号を所定の通倍比で周波数通倍したクロック信号を出力する周波数通倍回路とを有するクロック発生回路。

【請求項2】 上記周波数通倍回路は、上記第2のクロック信号と分周信号との位相を比較し、比較結果に応じて位相差信号を出力する位相比較回路と、

上記位相差信号に応じて所定のレベルを有する発振制御信号を出力する増幅回路と、

上記発振制御信号により設定した発振周波数で発振し、発振信号を上記通倍したクロック信号として出力する電圧制御発振回路と、

上記通倍したクロック信号を所定の分周比で分周し、分周信号を上記位相比較回路に出力する分周回路とを有する請求項1記載のクロック発生回路。

【請求項3】 入力クロック信号と分周信号の位相を比較し、上記入力クロック信号と上記分周信号の位相差に応じてレベルが変化する位相差信号を出力する位相比較回路と、

上記位相差信号に周波数制御信号のレベルに応じたバイアス電圧を加えた発振制御信号を出力する増幅回路と、

上記発振制御信号により設定した発振周波数で発振し、発振信号を出力する電圧制御発振回路と、

上記クロック信号を所定の分周比で分周し、分周信号を上記位相比較回路に出力する分周回路とを有するクロック発生回路。

【請求項4】 上記増幅回路は、一方の入力端子に上記位相差信号が入力され、他方の入力端子に上記周波数制御信号が入力される差動増幅回路により構成されている請求項3記載のクロック発生回路。

【請求項5】 上記位相比較回路からの位相差信号の高周波成分を減衰させ、低周波成分を抽出して、上記増幅回路に出力するローパスフィルタを有する請求項3記載のクロック発生回路。

【請求項6】 入力クロック信号と分周信号の位相を比較し、上記入力クロック信号と上記分周信号の位相差に応じた位相差信号を出力する位相比較回路と、

上記位相差信号および周波数制御信号に応じてチャージまたはディスチャージ電流を発生し、当該チャージまたはディスチャージ電流に応じて充放電するキャパシタから発振制御信号が出力するチャージポンプ回路と、

上記発振制御信号により設定した発振周波数で発振し、

クロック信号を出力する電圧制御発振回路と、

上記クロック信号を所定の分周比で分周し、分周信号を上記位相比較回路に出力する分周回路とを有するクロック発生回路。

【請求項7】 上記チャージポンプ回路は、上記位相比較回路からの位相差信号に応じて第1の電流を発生し、接続端子に出力する第1の電流発生回路と、

上記周波数制御信号に応じて第2の電流を発生し、上記接続端子に出力する第2の電流発生回路と、

10 一方の電極が上記接続端子に接続され、他方の端子が接地され、上記第1および第2の電流に応じて充電または放電することにより、上記接続端子の電圧を変化させ、当該接続端子の電圧を上記発振制御信号として上記電圧制御発振回路に供給するキャパシタとを有する請求項6記載のクロック発生回路。

## 【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は、電磁波輻射を低減するために変動する周波数を持つクロック信号を発生するクロック発生回路に関するものである。

【0002】

【従来の技術】 近年、半導体製造技術の進歩により半導体素子の最高動作可能な周波数は高くなる。例えば、一例としてパーソナルコンピュータに広く使用されているCPU（中央処理装置）の動作クロック周波数は、開発当初の10MHz前後からすでに200乃至300MHzに達した。このため、高速で動作可能な半導体装置が数多く実現されてきた。

【0003】

30 【発明が解決しようとする課題】 ところで、上述したように、半導体装置の動作周波数の向上によりもたらした問題の一つは電磁波輻射である。周波数の向上に伴い、高周波信号の波長が短くなり、接続回路または基板内部の配線長は高周波信号の波長とほぼ同じオーダーになると、基板内部の配線などの接続部はアンテナとして機能し、周囲への電磁波輻射が急激に増加してしまうという不利益がある。

【0004】 高速なクロック信号で動作する半導体素子を用いた電子機器の電磁波輻射により、電子機器間の相互干渉による誤動作、通信装置への妨害などをはじめ、人体への影響も懸念されている。現在電子輻射が問題となる電子機器に対して、回路の配置などを改良し電磁波輻射を低減するほか、電磁波遮蔽（シールド）により周囲への電磁波の漏れを低減させるなどの対策が施されている。しかし、モバイル機器などでは小型化、軽量化が要求された場合に、電磁波輻射を低減するためのシールドを十分に施すことができず、電磁波輻射に対する有効な防止方法はほとんどない。

【0005】 本発明は、かかる事情に鑑みてなされたものであり、その目的は、半導体装置の動作クロック信号

を微小に遷移させることにより、クロック信号のスペクトラム拡散を実現でき、電磁波輻射を低減可能なクロック信号を生成するクロック発生回路を提供することにある。

#### 【0006】

【課題を解決するための手段】上記目的を達成するため、本発明のクロック発生回路は、入力されたクロック信号を積分し、当該クロック信号の立ち上がりおよび立ち下がりにおける時間に対するレベル変化の傾きを緩やかにした積分クロック信号を出力する積分回路と、上記入力クロック信号より低い周波数でレベルを変化する周波数制御信号に応じて上記積分クロック信号をレベル制限し、周波数が上記周波数制御信号に従って変化する第2のクロック信号を出力するリミッタ回路と、上記第2のクロック信号を所定の通倍比で周波数通倍したクロック信号を出力する周波数通倍回路とを有する。

【0007】また、本発明では、好適には、上記周波数通倍回路は、上記第2のクロック信号と分周信号との位相を比較し、比較結果に応じて位相差信号を出力する位相比較回路と、上記位相差信号に応じて所定のレベルを有する発振制御信号を出力する増幅回路と、上記発振制御信号により設定した発振周波数で発振し、発振信号を上記通倍したクロック信号として出力する電圧制御発振回路と、上記通倍したクロック信号を所定の分周比で分周し、分周信号を上記位相比較回路に出力する分周回路とを有する。

【0008】また、本発明のクロック発生回路は、入力クロック信号と分周信号の位相を比較し、上記入力クロック信号と上記分周信号の位相差に応じてレベルが変化する位相差信号を出力する位相比較回路と、上記位相差信号に周波数制御信号のレベルに応じたバイアス電圧を加えた発振制御信号を出力する増幅回路と、上記発振制御信号により設定した発振周波数で発振し、クロック信号を出力する電圧制御発振回路と、上記クロック信号を所定の分周比で分周し、分周信号を上記位相比較回路に出力する分周回路とを有する。

【0009】さらに、本発明のクロック発生回路は、入力クロック信号と分周信号の位相を比較し、上記入力クロック信号と上記分周信号の位相差に応じた位相差信号を出力する位相比較回路と、上記位相差信号および周波数制御信号に応じてチャージまたはディスチャージ電流を発生し、当該チャージまたはディスチャージ電流に応じて充放電するキャパシタから発振制御信号が出力するチャージポンプ回路と、上記発振制御信号により設定した発振周波数で発振し、クロック信号を出力する電圧制御発振回路と、上記クロック信号を所定の分周比で分周し、分周信号を上記位相比較回路に出力する分周回路とを有する。

【0010】本発明によれば、クロック発生回路において、半導体装置の正常の動作に影響しない程度にわずか

に周波数が遷移するクロック信号を発生し、動作クロック信号として半導体装置に供給することにより、クロック信号の周波数スペクトラムを拡散させ、半導体装置の電磁波輻射を低減させる。具体的に、例えば、入力クロック信号に比べて緩やかにレベルが変化する周波数制御信号より、積分したクロック信号をリミットすることで、周波数が変化するクロック信号が生成され、当該クロック信号に応じて、PLL回路により所定の通倍数で通倍したクロック信号を生成し半導体装置に供給する。

【0011】また、本発明のクロック発生回路はPLL回路により構成され、当該PLL回路においてVCOに供給する制御信号を発生する直流増幅回路、例えば、差動増幅回路において、一方の入力端子に位相比較回路が入力され、他方の入力端子に周波数制御信号が入力されるので、VCOに入力される発振制御信号に発振周波数に応じたバイアス成分が含まれ、当該周波数制御信号に応じてVCOの発振周波数が遷移するように制御される。さらに、PLL回路を構成するチャージポンプにおいて、周波数制御信号に応じてバイアス電圧が発生され、位相差信号に応じて発生した電流に当該バイアス電流が加えられるので、チャージポンプの出力信号により発振周波数が制御されるVCOの発振周波数は周波数制御信号に従って遷移する。

#### 【0012】

##### 【発明の実施の形態】第1実施形態

図1は本発明に係るクロック発生回路の第1の実施形態を示す回路図である。本実施形態のクロック発生回路は、積分器1、リミッタ2、PLL回路3および分周器4により構成されている。

【0013】積分器1は、入力されたクロック信号CKINを積分して、積分したクロック信号CKSを出力する。リミッタ2は、積分クロック信号CKSおよび周波数制御信号SCを受けて、これらの信号に応じてPLL回路3に入力するクロック信号SINを出力する。PLL回路3は、リミッタ2から入力されたクロック信号SINおよび分周器4から入力された分周信号SDに応じて、例えば、クロック信号SINに応じて周波数或いは位相が制御されるクロック信号CKOUTを出力する。

【0014】リミッタ2に入力される周波数制御信号SCに応じて、PLL回路3の出力クロック信号CKOUTの出力を微小の変動幅をもって遷移させることにより、クロック信号CKOUTのスペクトラムを拡散させる。このため、クロック信号CKOUTを動作周波数として動作する半導体装置においては、動作クロック信号のスペクトラムが分散した結果、電磁波輻射の低減を実現できる。

【0015】図2は、分周器を含むPLL回路3の一構成例を示している。図示のように、PLL回路3は、位相比較器10、ローパスフィルタ(LPF)20、直流増幅器30、電圧制御発振器(VCO)40および分周

器50により構成されている。なお、図2における分周器50は、図1に示す分周器4と同一のものである。

【0016】位相比較回路10は、分周回路50からの分周信号 $S_D$ とリミッタ2から入力されたクロック信号 $S_{IN}$ との位相を比較し、これらの信号の位相差を示すアップダウン信号 $S_{UD}$ を出力する。ローパスフィルタ20は、位相比較器10からのアップダウン信号 $S_{UD}$ に含まれている高周波成分を除去し、低周波成分のみからなる信号 $S_L$ を出力する。直流増幅器30は、図示のように、差動増幅器AMPおよび抵抗素子 $R_1$ 、 $R_2$ からなる反転型増幅回路であり、ローパスフィルタ20からの低周波信号 $S_L$ を増幅し、さらに増幅した信号に所定の直流レベル $V_{dc}$ を加えた信号 $S_V$ を制御信号としてVCO40に出力する。VCO40は、直流増幅器30からの制御信号 $S_V$ により制御された発振周波数で発振し、発振信号を出力する。なお、VCO40により出力される発振信号は、動作クロック信号 $CK_0$ として他の半導体装置に供給される。分周器50は、VCO40からのクロック信号 $CK_0$ を予め設定された分周比で分周し、分周信号 $S_D$ を位相比較器10に出力する。

【0017】図3は、本実施形態のクロック発生回路の各部分回路の信号波形を示している。以下、図1～図3を参照しつつ、本実施形態のクロック発生回路の動作について説明する。

【0018】図1のリミッタ2に入力される周波数制御信号 $S_C$ は、図3(a)に示すように、例えば、所定の周期を持つ三角波である。当該三角波は、入力クロック信号 $CK_{IN}$ よりかなり周波数が低く、緩やかに変化する低周波の信号である。なお、ここで、一例として三角波の信号を示しているが、周波数制御信号 $S_C$ は、三角波に限定されるものではなく、他の信号、例えば、正弦波、或いは階段状にレベルが変化する信号でもよい。

【0019】図3(b)に示す一定の周期 $T$ を持つクロック信号 $CK_{IN}$ は、積分器1に入力され、積分の結果、同図(c)に示す積分クロック信号 $CK_S$ が得られる。リミッタ2において、周波数制御信号 $S_C$ を用いて、積分クロック信号 $CK_S$ のレベルをリミットした結果、同図(d)に示す周期が絶えずに変化するクロック信号が得られる。当該クロック信号は入力信号 $S_{IN}$ としてPLL回路3に供給される。

【0020】PLL回路3は、分周器4の分周比 $n$  ( $n$ は正整数)で設定した通倍数で入力信号 $S_{IN}$ の周波数を通倍し、クロック信号 $CK_0$ を発生する。例えば、入力信号 $S_{IN}$ の周波数を $f$ とすると、出力クロック信号 $CK_0$ の周波数は $nf$ となる。入力信号 $S_{IN}$ の周波数が変化し、例えば、 $(f + \Delta f)$ になると、出力クロック信号 $CK_0$ の周波数もそれに追従して、 $(nf + n\Delta f)$ に変化する。上述したように、リミッタ2において周波数制御信号 $S_C$ に応じて積分クロック信号 $CK_S$ をリミットの結果、得られた信号 $S_{IN}$ の周波数は、周波数制御信

号 $S_C$ のレベルに応じて制御される。このため、PLL回路3の出力クロック信号 $CK_0$ の周波数も制御信号 $S_C$ のレベルにより制御される。即ち、本実施形態のクロック発生回路は、一種の周波数変調回路として機能し、周波数制御信号 $S_C$ を用いて入力クロック信号 $CK_{IN}$ の周波数に対して変調機能を働き、周波数が変化するクロック信号 $CK_0$ を提供することができる。

【0021】本実施形態のクロック発生回路により、周波数制御信号 $S_C$ に応じて周波数が変化するクロック信号 $CK_0$ が発生される。当該クロック信号 $CK_0$ を動作クロック信号として動作する他の半導体装置において、クロック信号のスペクトラムが拡散されるので、電磁波輻射を大幅に低減することが可能である。図4(b)はスペクトラム拡散が施されたクロック信号のスペクトラムを示している。なお、比較のため、同図(a)にはスペクトラム拡散が行われていないクロック信号 $CK$ のスペクトラムを示している。

【0022】図4(a)に示すように、スペクトラム拡散が行われていない場合に、クロック信号 $CK$ のスペクトラムは、ノイズ成分などによりわずかに両側に広がった部分を除けば、ほとんど中心周波数 $f_{CK}$ に集中している。これに対して、本実施形態のクロック発生回路によりスペクトラムが拡散したクロック信号のスペクトラムは、同図(b)に示すように、周波数 $f_{CK}$ を中心に広範囲に両側に広がり、そのピーク値は、図(a)に示すスペクトラムに比べて大幅に低減される。これによって、本実施形態のクロック発生回路で供給したクロック信号 $CK_0$ で動作する半導体装置において、電磁波輻射が大幅に低減することが可能となり、シールドなどの対策を講じることが困難な場合でも、装置周辺への電磁波の漏れを大幅に減少させることが可能である。

#### 【0023】第2実施形態

図5は本発明に係るクロック発生回路の第2の実施形態を示す回路図である。上述したクロック発生回路の第1の実施形態において、リミッタを用いてレベルが緩やかに変化する周波数制御信号 $S_C$ で積分したクロック信号のレベルをリミットすることで周波数が遷移するクロック信号を発生し、当該クロック信号を所定の通倍比で通倍したクロック信号 $CK_0$ を発生する。このため、リミッタの他に積分器が必要であり、PLL回路以外の付加回路が多く、回路のコストが大きくなる。

【0024】これに対して、本実施形態のクロック発生回路において、PLL回路のみを用いて周波数を遷移させることができ、簡単な回路構成により所望のクロック信号を発生することができ、小型化、安価なクロック発生回路を実現できる。以下、図5を参照しつつ、本実施形態のクロック発生回路の構成およびその動作について説明する。

【0025】図5に示すように、本実施形態のクロック

発生回路を構成するPLL回路は、図2に示すPLL回路3とほぼ同じ構成を有する。ただし、本実施形態において、直流増幅器30aを構成する差動増幅AMPにレベルが変化する周波数制御信号SC1が入力され、これによって直流増幅器30aから出力される制御信号SVのレベルを制御し、VCO40の発振周波数を制御する。

【0026】PLL回路を構成する位相比較器10には、クロック信号SINおよび分周器50からの分周信号SDが入力される。クロック信号SINは、例えば、安定した周波数を持つ基準クロック信号である。位相比較器10は、入力されたクロック信号SINと分周信号SDとの位相を比較し、これらの信号の位相差に応じてアップダウン信号SUPを出力する。ローパスフィルタ20は、位相比較器10からのアップダウン信号SUPに含まれている高周波成分を除去し、低周波成分のみからなる信号SLを出力する。

【0027】直流増幅器30aは、例えば、差動増幅器AMPにより構成され、ローパスフィルタ20からの低\*

$$V_L = (V_{dc} + \Delta V) - (V_S - V_{dc} - \Delta V) \cdot R_1 / R_2 \\ = (V_{dc} + \Delta V) (R_1 + R_2) / R_2 - V_S R_1 / R_2 \quad \dots (1)$$

【0030】VCO40は、直流増幅器30aから出力される制御信号SVにより、発振周波数が制御され、当該発振周波数を持つクロック信号CK0が出力される。このため、VCO40の発振周波数は、直流増幅器30aに入力された周波数制御信号SC1のレベル変化に応じて遷移する。即ち、出力クロック信号CK0のスペクトラムが拡散される。

【0031】このように、差動増幅回路AMPにバイアス信号SC1を加えた結果、ローパスフィルタ20の出力信号SLの電圧レベルが式(1)に示す電圧VLになるようにPLL回路が動作する。その結果、差動増幅回路AMPに加えられたバイアス信号SC1のレベルに応じてVCO40の発振周波数が変化する。

【0032】クロック信号CK0が動作クロック信号として、他の半導体装置が供給されるので、当該クロック信号CK0で動作する半導体装置の電磁波放射が大幅に低減される。

【0033】以上説明したように、本実施形態によれば、PLL回路において位相比較器10により入力した基準クロック信号SINと分周器50からの分周信号SDとの位相を比較し、これらの信号の位相差に応じてアップダウン信号SUPを出力し、ローパスフィルタ20はその高周波成分を除去し、低周波成分からなる信号SLを出力する。直流増幅器30aは入力される周波数制御信号SC1をバイアスとする制御信号SVを生成し、VCO40に供給する。VCO40は制御信号SVにより設定した周波数で発振し、周波数制御信号SC1に応じて周波数が遷移するクロック信号CK0を発生し、動作クロック信号として半導体装置に供給するので、スペクトラム拡散したクロック信号で動作する半導体装置の電磁波輻

\*周波数信号SLが抵抗素子R1を通して差動増幅器AMPの反転入力端子“-”に入力され、さらに、当該反転入力端子“-”は抵抗素子R2を介して差動増幅器AMPの出力端子に接続されている。差動増幅器AMPの入力端子“+”に周波数制御信号SC1が入力される。図示のように、周波数制御信号SC1は直流レベルVdcにバイアス電圧ΔVが加わった信号であり、例えば、図3(a)に示す三角波である。

【0028】このように、差動増幅器AMPおよび抵抗素子R1、R2により反転増幅回路が構成され、その出力端子から入力信号SLの反転信号にバイアス信号SC1が加わった信号SVが出力され、VCO40に供給される。ここで、ローパスフィルタ20の出力信号SLの電圧をVLとし、信号SVの電圧をVSとすると、次式が成り立つ。

【0029】

【数1】

射を低減できる。

【0034】第3実施形態

図6は本発明に係るクロック発生回路の第3の実施形態を示す回路図である。図示のように、本実施形態のクロック発生回路は図5に示した本発明の第2の実施形態とほぼ同様に、PLL回路を用いて周波数が遷移するクロック信号を発生する。ただし、本実施形態において位相比較器10aの出力信号に応じて動作するチャージポンプ60に周波数制御信号SC2で所定のバイアス電流を発生させることにより、信号SLのレベルを制御することで、VCO40の発振周波数を制御する。

【0035】位相比較器10aに入力される信号SINは、例えば、所定の周波数を持つ基準クロック信号である。位相比較器10aは、当該基準クロック信号SINと分周器50からの分周信号SDの位相を比較し、比較結果に応じてアップ信号SUPまたはダウン信号SDWを出力する。なお、これらの出力信号は、例えば、基準クロック信号SINと分周信号SDの位相差に応じて幅が制御されるパルス信号である。例えば、基準クロック信号SINが分周信号SDより位相が進んでいるとき、これらの信号の位相差に応じた幅を持つパルス信号であるアップ信号SUPが出力され、逆に、基準クロック信号SINが分周信号SDより位相が遅れているとき、これらの信号の位相差に応じた幅を持つパルス信号であるダウン信号SDWが出力される。

【0036】チャージポンプ60は、アップ信号SUPまたはダウン信号SDWに応じてチャージ電流icを発生する。さらに、入力された周波数制御信号SC2に応じてバイアス電流Δicを発生し、チャージ電流icに加える。このため、チャージ電流icおよびバイアス電流Δ

$i_C$  の和 ( $i_C + \Delta i_C$ ) に応じて、キャパシタC1が充電または放電し、当該キャパシタC1の充放電に応じてレベルが制御される信号 $S_L$ が出力される。

【0037】直流増幅器30は、チャージポンプ60から出力される信号 $S_L$ を増幅し、得られた信号 $S_V$ を制御信号としてVCO40に供給する。なお、本実施形態の直流増幅器30は、例えば、図2に示すPLL回路3を構成する直流増幅器と同じ構成を有するものでよい。VCO40は、制御信号 $S_V$ により制御された発振周波数で発振し、発振信号を出力する。当該発振信号を動作

クロック信号CK0として、半導体装置に供給する。分周器50はVCO40で発生したクロック信号CK0を予め設定した分周比 $n$ で分周し、分周信号 $S_D$ を発生し、位相比較器10aに入力する。

【0038】図7はチャージポンプ60の一構成例を示す回路図である。図示のように、チャージポンプ60は、電源電圧 $V_{dd}$ と接地電位GND間に直列に接続されているpnpトランジスタP1とnpnトランジスタQ1およびpnpトランジスタP2とnpnトランジスタQ2、さらに、これらのトランジスタのエミッタ側に接続されている抵抗素子R3、R4、R5およびR6により構成されている。

【0039】トランジスタP1のエミッタが抵抗素子R3を介して電源電圧 $V_{dd}$ に接続され、ゲートに位相比較器10aからのアップ信号 $S_{UP}$ が入力される。トランジスタQ1のエミッタが抵抗素子R4を介して接地され、ゲートに位相比較器10aからのダウン信号 $S_{DW}$ が入力される。トランジスタP1とQ1コレクタはノードND1に接続されている。トランジスタP2のエミッタが抵抗素子R5を介して電源電圧 $V_{dd}$ に接続され、コレクタがノードND1に接続されている。トランジスタQ2のエミッタが抵抗素子R6を介して接地され、コレクタがノードND1に接続されている。さらに、トランジスタP2とQ2のゲートに周波数制御信号 $S_{C2}$ が入力されている。キャパシタC1は、ノードND1と接地電位GNDとの間に接続されている。

【0040】位相比較器10aからアップ信号 $S_{UP}$ 、例えば、ローレベルのパルス信号が入力されると、トランジスタP1に電流 $I_1$ が流れ、ノードND1に入力される。一方、位相比較器10aからダウン信号 $S_{DW}$ 、例えば、ハイレベルのパルス信号が入力されると、トランジスタQ1に電流 $I_2$ が流れる。キャパシタC1は、ノードND1に電流 $I_1$ が入力されるとき、当該電流により充電され、ノードND1の電位が上昇する。逆に、ノードND1からトランジスタQ2に電流 $I_2$ が流れると、ノードND1がディスチャージされ、ノードND1の電位が降下する。このため、位相比較器10aの比較結果に応じて、キャパシタC1が充電またはディスチャージされ、ノードND1の電圧が制御される。

【0041】一方、トランジスタP2とQ2のゲートに

入力された周波数制御信号 $S_{C2}$ のレベルに応じて、これらのトランジスタに流れる電流が制御される。例えば、周波数制御信号 $S_{C2}$ のレベルが低くなると、トランジスタP2に電流 $I_3$ が流れて、これに応じてキャパシタC1が充電される。一方、周波数制御信号 $S_{C2}$ のレベルが高くなると、トランジスタQ2に電流 $I_4$ が流れ、これに応じてキャパシタC1はディスチャージされる。このため、周波数制御信号 $S_{C2}$ のレベルに応じて、キャパシタC1が充電またはディスチャージされ、ノードND1の電圧が制御される。

【0042】上述したように、チャージポンプ60において、位相比較器10aからのアップ信号 $S_{UP}$ またはダウン信号 $S_{DW}$ および周波数制御信号 $S_{C2}$ に応じて、ノードND1の電圧、即ち、チャージポンプ60の出力信号 $S_L$ のレベルが制御される。当該信号 $S_L$ は直流増幅器30により増幅したあと制御信号 $S_V$ としてVCO40に入力される。この結果、VCO40の発振周波数は位相比較器10aからのアップ信号 $S_{UP}$ およびダウン信号 $S_{DW}$ のほか、周波数制御信号 $S_{C2}$ により制御される。

【0043】チャージポンプ60に入力される周波数制御信号 $S_{C2}$ は、例えば、図3(a)に示す三角波とすると、VCO40の出力クロック信号CK0は、当該三角波のレベル変化に応じて周波数が緩やかに遷移する。このため、クロック信号CK0を動作クロックとする半導体装置において、クロック信号のスペクトラムが拡散するので、電磁波放射が大幅に低減される。

【0044】以上説明したように、本実施形態によれば、位相比較器10aは入力された基準クロック信号 $S_{IN}$ と分周器50からの分周信号 $S_D$ の位相を比較し、これらの信号の位相差に応じてアップ信号 $S_{UP}$ またはダウン信号 $S_{DW}$ を出力する。チャージポンプ60は位相比較器10aの出力信号および周波数制御信号 $S_{C2}$ に応じて充電またはディスチャージ電流を発生し、キャパシタC1はこれに応じて充電またはディスチャージし、信号 $S_L$ のレベルを制御する。直流増幅器30により信号 $S_L$ を増幅して制御信号 $S_V$ を生成し、VCO40に供給し、VCO40は制御信号 $S_V$ で設定した周波数で発振し、クロック信号CK0を出力するので、当該クロック信号CK0の周波数は周波数制御信号 $S_{C2}$ のレベル変化に応じて遷移し、スペクトラムが拡散するのでこれを動作クロックとする半導体装置の電磁波放射が大幅に低減される。

【0045】

【発明の効果】以上説明したように、本発明のクロック発生回路によれば、発生されるクロック信号の周波数が緩やかに遷移させることにより、そのスペクトラムが拡散し、これに応じて動作する半導体装置の電磁波放射が低減できる利点がある。

【図面の簡単な説明】

【図1】本発明に係るクロック発生回路の第1の実施形

態を示す回路図である。

【図2】図1に示すクロック発生回路を構成するPLL回路の一構成例を示す回路図である。

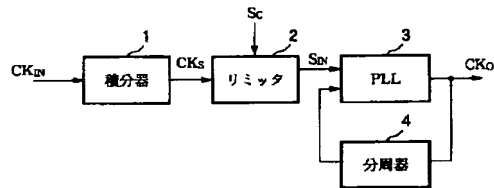
【図3】第1の実施形態のクロック発生回路の動作を示す波形図である。

【図4】クロック信号のスペクトラムを示す図である。

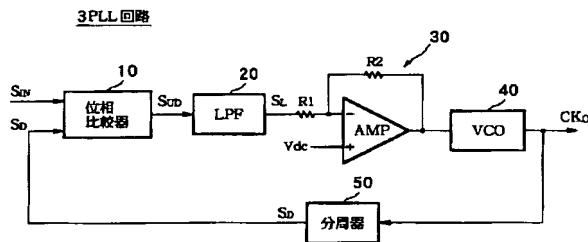
【図5】本発明に係るクロック発生回路の第2の実施形態を示す回路図である。

【図6】本発明に係るクロック発生回路の第3の実施

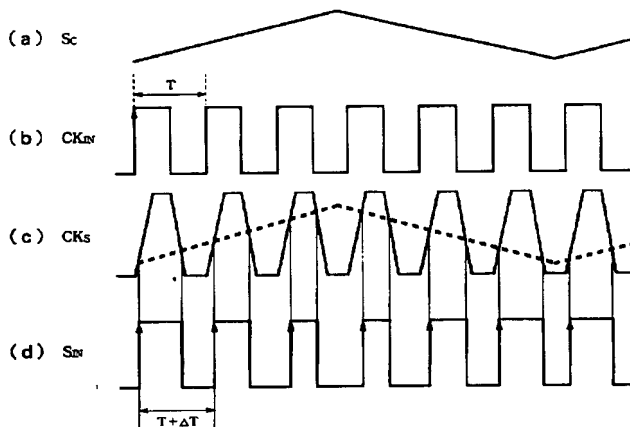
【図1】



【図2】



【図3】



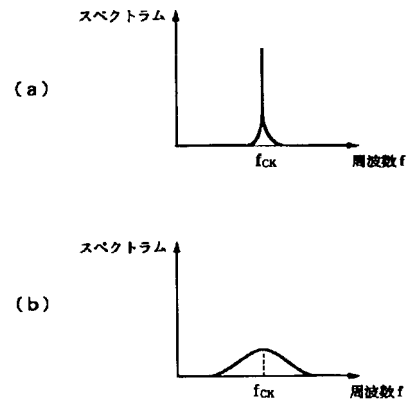
態を示す回路図である。

【図7】図6に示すクロック発生回路を構成するチャージポンプの一構成例を示す回路図である。

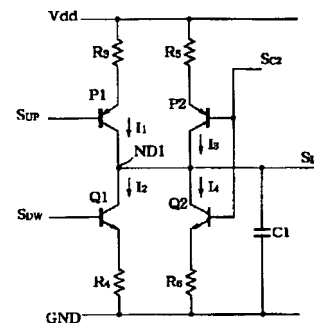
【符号の説明】

1…積分器、2…リミッタ、3…PLL回路、4…分周器、10、10a…位相比較器、20…ローパスフィルタ、30、30a…直流増幅器、40…VCO、50…分周器、60…チャージポンプ、Vdd…電源電圧、GND…接地電位。

【図4】

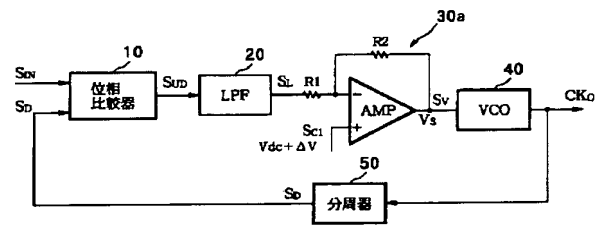


【図7】

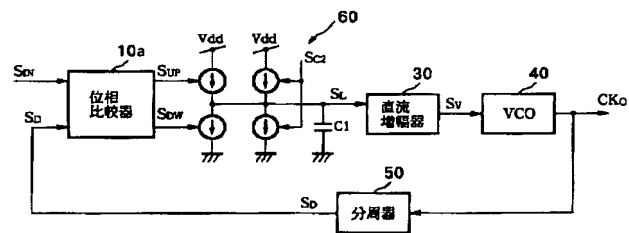




【図5】



【図6】



I, Motoko FUJITA, of Fujitsu Limited, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588 Japan, hereby certify that, to the best of my knowledge and belief, the following is a true translation made by me (or compared by me), and for which I accept responsibility, of Japanese Patent Application No. 2002-266631.

Motoko Fujita  
Signature

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**[Scope of Patent Claims]**

**[Claim1]**

Regarding the clock generator circuit equipped with the phase comparator which is inputted by a standard clock and operating clock and a voltage control oscillator that generated the aforementioned operating clock based on the output signal of the aforementioned phase comparator, the clock generator circuit has the characteristics wherein the aforementioned voltage control oscillator comprises of a voltage current converter that converts the voltage signal into an current signal, an variable current circuit which can fluctuate the aforementioned current signal and an current control oscillator that oscillates the frequencies based on the aforementioned variable current signals.

**[Claim2]**

A clock generator circuit as mentioned in Claim 1 that is characterized by the presence of the aforementioned variable current circuit, which could be a current D/A converter or a current D/A converter with low pass filter.

**[Claim 3]**

It is a clock generator circuit wherein the results of comparison between the standard clock the comparison clock are converted to current signals and based on the aforementioned current signals, the operation clock is generated, and furthermore, the characteristics of the aforementioned clock generator circuit is equipped with Circuit No 1 that generate multiple current signals by changing the aforementioned current signal and Circuit No 2 which generates clocks with multiple varying frequencies based on the aforementioned multiple current signals.

**[Claim 4]**

A clock generator that is characterized by the presence of a phase comparator which outputs The results of comparison between the standard clock and the comparison clock, and Circuit No 1 that generates current signals based on the results of the aforementioned comparison as well as Circuit No. 2 that Generates current Signal No. 1 and Current signal No. 2 based on the aforementioned current signal. Further the clock generator circuit also is equipped with a 3<sup>rd</sup> circuit that generates a 2<sup>nd</sup> frequency clock based on the aforementioned 2<sup>nd</sup> current signal along with the generation of the clock with the first frequency based on the aforementioned 1<sup>st</sup> Current signal:

**[Claim 5]**

Regarding A clock generator circuit which is equipped with the 1<sup>st</sup> clock generator part that generates the 1<sup>st</sup> clock, and the 2<sup>nd</sup> clock generator part that generates the 2<sup>nd</sup> clock, wherein the 1<sup>st</sup> clock generator part is equipped with the phase comparator which compares the standard clock and the operating clock and a voltage current converter that converts the signal based on the aforementioned comparison results or the comparison results into current signals as well as the as the 1<sup>st</sup> voltage control oscillator that generated the 1<sup>st</sup> operating clock based on the aforementioned current signal. Further the 2<sup>nd</sup> clock generator part comprises of the variable current circuit that can convert the aforementioned current signals and the 2<sup>nd</sup> current control oscillator that oscillates the frequency clock based on the aforementioned variable current signal.

**[Claim 6]**

Regarding the clock generator circuit that generated a 1<sup>st</sup> clock of a frequency spectrum containing N number of peaks (N is an integer that is greater than 1A), the clock generator circuit is characterized by the presence of the methods as follow: on the basis of the current signal which is generated by the comparison results obtained between the standard clock and the comparison clock, it is equipped with a method to generate the 2<sup>nd</sup> clock containing a frequency spectrum with M number of peaks (N is an integer that is greater than 1,  $M > N$ ).

**[Claim 7]**

Regarding PLL that is equipped with a phase comparator that inputs a standard clock and an operating clock and, a charge pump that supplies the output of the aforementioned charge pump, and a voltage control oscillator that outputs the aforementioned operating clock along with the supply of output of the aforementioned charge pump, the characteristics of PLL is that the above mentioned voltage control oscillator is equipped with a voltage current converter that converts the voltage signal into the current signal, an current variable current circuit that can change the aforementioned current signal and a current control oscillator that oscillates the frequency based on the aforementioned variable current signal.

**[Claim 8]**

Regarding the operation clock generation method, the characteristics of operation clock generation method is that the standard clock and the comparison clock are compared and the results of the aforementioned comparison is converted into current signals, the aforementioned current signals are changed based on the control signal, and the operating clock with varying frequencies is outputted based on the above mentioned variable current signal.

**[Claim 9]**

A operation clock generation mechanism is characterized by comparing the standard clock and the comparison clock, converting the results of the aforementioned comparison into current signals, generating the 1<sup>st</sup> current signal and the 2<sup>nd</sup> current signal basing the above mentioned current signal on the control signal, and then generating the 1<sup>st</sup> frequency clock based on the aforementioned 1<sup>st</sup> current signal and also generating the 2<sup>nd</sup> frequency clock based on the aforementioned 2<sup>nd</sup> current signal.

**[Claim 10]**

A clock generator circuit is characterized by comparing the standard clock and the comparison clock, and generating multiple current signals on the basis of the aforementioned results of comparison and further generating a clock with frequency spectrum containing M number of peaks (M is an integer that is greater than 2) based on the aforementioned current signals.

**[Detailed explanation of the invention]****[0001]****[Technical field of the present invention]**

The present invention is related to a clock generator circuit that generates an operating clock of a semi conductor device and is in particular related to a clock generator device that can reduce electromagnetic bandwidth radiation by achieving the diffusion of the spectrum.

**[0002]**

**[Prior art and technology]**

Due to the increased capacity of the semi conductor, the operating clock of the semi conductor equipment (operating frequency) has been greatly increased and improved over the past few years. This has been accompanied by the problem caused by the impact of the electromagnetic bandwidth radiation by the clock generator circuit on the surrounding circuits.

**[0003]**

Figure 1 shows the traditionally used clock generator circuit, PLL (Phase Locked Loop).

**[0004]**

PLL 1 oscillates by generating the semi conductor equipment's operating clock.

**[0005]**

PLL 1 is made up of 1/N frequency divider 2, phase comparator 3. Charge pump 4, loop filter 5, VCO (voltage control oscillator) 6, and 1/M frequency divider device 9.

**[0006]**

The standard clock RCLK is supplied to the 1/N frequency divider 2 and is divided into 1/N times (N is an integer), and is then supplied to the phase comparator 3. The signal generated in VCO 6 is divided into 1/M times (M is an integer) after supplying it to the 1/M frequency divider 7 and is then supplied to the phase comparator 3. In the phase comparator 3, the standard clock RCLK which has been divided into 1/N times as well as the signals which have been divide into 1/M times are compared and the comparison signal corresponding to the compared phase difference is provided to the charge pump 4.

**[0007]**

The charge pump 4 supplies the signal that is based on the comparison signal to the loop filter 5. The loop filter removes all the noise etc of the high frequency components and after smoothing them out; the signals are supplied to VCO6.

**[0008]**

Based on the smoothened signal that has been outputted from the loop filter 5, VCO 6 outputs the operating clock CLK. This operating clock CLK is M/N times the standard clock RCLK.

**[0009]**

In such a manner, PLL1 generates the operating clock CLK with specified frequency that was generated based on the standard clock RCLK and then oscillate the clock.

**[0010]**

However, in order that the frequency keeps oscillating with specified operation clock, a problem occurs in PLL 1 wherein the electromagnetic waves that are radiated from PLL1 are very large and have a tremendous impact on the surrounding electronic devices.

**[0011]**

Figure 2 shows the frequency spectrum of the clock that is oscillated by PLL1 in diagram 1.

**[0012]**

When the PLL 1 is operated such that the specified operation clock (for example, 16 MHz) oscillates, the oscillation frequency spectrum shows a very large peak value as has been shown in Figure 2 and due to this, the electromagnetic waves that are radiated from PLL 1 also gets extremely large. The maximum electromagnetic radiation may cause the malfunctioning and errors in operation of other electronic devices and as there is a possibility of these affecting human beings as well, this poses a grave problem.

**[0013]**

The same problem also arises in the PLL oscillator as described in Patent Publication 1995-143001.

**[0014]**

**[Methods and operating effects in order to solve the problems]**

In order to solve the above mentioned problems, regarding the clock generator circuit which is equipped with a standard clock and an operation clock that are inputted in the phase comparator as well as a voltage control oscillator that generates the above mentioned operation clock based on the output signal of the aforementioned phase comparator, this invention provides the clock generation circuit with the characteristics wherein the aforementioned voltage control oscillator is equipped with a voltage control oscillator that converts the voltage signal to a current signal and the current variable current circuit that can convert the aforementioned current signal and also the voltage control oscillator that oscillates the frequency based on the aforementioned variable current signal.

**[0015]**

Figure 3 is the logical diagram of this invention.

**[0016]**

The clock generation circuit in this invention is composed in such a way that it can fluctuate the oscillation frequency.

**[0017]**

The clock generator circuit 8 is comprised from the  $1/N$  frequency divider 9, the phase comparator 10, the charge pump 11, the loop filter 12, VCO (voltage control oscillator) 13, and the  $1/M$  frequency divider 17 and apart from the composition of the VCO, it is the same as the traditionally used PLL that has been shown in Figure 1.

**[0018]**

The VCO 13 is constituted from V-I converter (voltage current converter) 14 and current variable current circuit 15 as well as an ICO (current control oscillator) 16.

**[0019]**

The V-I converter 14 converts the voltage signal from the charge pump 11 to the current signal. The current variable current circuit 15 changes the converted current signal and ICO 16 oscillates the frequency corresponding to the current signal that was fluctuated.

**[0020]**

In this fashion, in the present invention, the oscillation frequency is fluctuated by changing the current signal that controls the oscillator frequency by using the current variable circuit.

**[0021]**

Using the clock generation circuit pertaining to the present invention, the following results may be obtained.

- (1) The oscillation frequency spectrum is effectively diffused and it enables to reduce the electromagnetic radiation.

**[0022]**

By fluctuating the frequency oscillated by the clock generation circuit, it enables to disperse the peak of the oscillation frequency spectrum.

**[0023]**

Figure 4 shows the frequency spectrum -1 that is oscillated by the present invention's clock generation circuit.

**[0024]**

In diagram 4, the unique peak of the traditional PLL frequency spectrum as has been shown in Figure 2 gets dispersed into multiple peaks and along with this, each of the peak values become smaller leading to the reduction in the electromagnetic waves that are radiated from the clock generation circuit.

As a result, it enables to avoid the impact to other electronic devices caused by the electromagnetic radiation from the clock generator device.

**[0025]**

Figure 5 shows the frequency spectrum -2 which is oscillated by the present inventions' clock generation circuit.

**[0026]**

Figure 5 (2) shows the further dispersion of the frequency spectrum, which is oscillated by the clock generation circuit as has been shown in Figure 4.

The peak of the spectrum almost vanishes and becomes fixed. Further, the unique peak value of the traditional PLL frequency spectrum (1) as has been shown in figure 2 is reduced drastically (X is reduced greatly). As a result, the electromagnetic waves that are radiated from the clock generator circuit are dramatically reduced.

- (2) The degree of dispersion of the oscillation frequency spectrum can be set freely.

**[0027]**

By fluctuating the current signal which controls the oscillation frequency based on the control signal, it enables to freely control the timing and the volume that fluctuates the clock generator circuit's oscillation frequency.

As a result, we can realize the spectrum dispersion of the desired oscillation frequency And a reduction in the electromagnetic radiation can be achieved as desired. In particular, in The VCO by making use of the IDAC (current D/A converter) also enables to digitally control the change of the oscillation frequency. In other words, by merely changing the input pattern to the IDAC, the degree of spectrum dispersion can be controlled and the control becomes greatly simplified.

- (3) An accurate transition of the oscillation frequency can be realized.



**[0028]**

In the VCO, on account of making use of the IDAC (current D/A converter), the impact of the parasitic volume is made difficult to receive, which in turn enables the precision of the transition of the oscillation frequency.

(4) It is now possible to effectively handle the dispersion that arises due to the fluctuation in the process, fluctuation in temperature and a fluctuation in the power source voltage.

**[0029]**

Based on the current from the V-I converter (voltage current converter), in other words, using the control current when the PLL is in a locked state as the base current, the IDAC in the VCO change the current signal which controls the oscillation frequency. Due to this, the clock generator circuit cannot be impacted easily by the dispersion caused by the fluctuations in process, fluctuations in temperature and fluctuations in power source voltage.

**[0030]**

For example, the input current of the ICO is 10mA and this oscillates at 10MHz. When PLL is in a locked state at 10MHz, and the input current of the IDAC fluctuates by  $\pm 1\%$ , the current input fluctuates within the ranges of 9.9 mA~10.1mA and the oscillation frequency fluctuates within the ranges of 9.9MHz~10.1MHz. In such a case, by the process fluctuations, temperature fluctuations and power source voltage fluctuations, when the ICO has an input current of 20mA, it is assumed that it ends up with 10MHz oscillation. IDAC fluctuates input current by  $\pm 1\%$  using the standard of input current of 20mA, the current input fluctuates anywhere between the ranges of 19.8 mA~20.2 mA and the oscillation frequency fluctuates within the 9.9MHz~10.1MHz range. In other words, since the range of fluctuation is the same as when there is no fluctuation in the process, temperature fluctuations or fluctuation in power source voltage, the impact from process fluctuation, temperature fluctuations or fluctuations in power source voltage fluctuation cannot be seen.

**[0031]**

On the one hand, the IDAC in the VCO does not depend on the current from the V-I converter (voltage current converter). In other words, based on a fixed standard current, the current signal which controls the oscillation frequency is assumed to be changed. When PLL is in a locked state at 10MHz, and if IDCA fluctuates the input current by  $\pm 1\%$ , the current input fluctuates anywhere between 9.9mA~10.1mA while the oscillation frequency fluctuates in the ranges between 9.9MHz~10.1MHz. This is the same as the IDAC that modifies the current signal based on the current from the V-I converter (voltage current converter). In such a case, on account of the process fluctuation, temperature fluctuations or fluctuations in power source voltage, it is assumed that ICO ends up oscillating at 10MHz when it has a current input of 20mA.

Since IDAC fluctuates input current by around  $\pm 1\%$  using the standard of the fixed input current 10mA the current input fluctuates anywhere between the ranges of 9.9 mA~ 10.1mA while the oscillation frequency fluctuates within 9.95MHz ~10.05MHz.

Comparing this to the case when there are no process fluctuation, temperature fluctuations or fluctuations in power source voltage, we find that the range of fluctuation is decreased to  $\pm 0.5\%$  and the impact from process fluctuation, temperature fluctuations or fluctuations in power source voltage becomes greater.

**[0032]**

Consequently, by making use of the IDAC by changing the current signal that controls the oscillation frequency based on the current from the V-I converter (voltage current converter), it enables to control the dispersion generated by the process fluctuation, temperature fluctuations or fluctuations in power source voltage.

**[0033]**

**[Embodiment form of the present invention]**

**[Working example 1 of the present invention]**

Figure 6 shows the Working example 1 of the present invention

**[0034]**

The PLL 18 in the current invention's working example 1 is equipped with the IDAC (current D/A converter) as the current variable circuit and changes the oscillation frequency.

**[0035]**

The PLL 18 as shown in Figure 6 is composed from 1/N frequency divider 19, phase comparator 20, charge pump 21, loop filter 22, VCO (voltage control oscillator) 23, and 1/M frequency divider 28 and apart from the structure of the VCO, it is the same as the traditional PLL as has been shown in figure 1.

**[0036]**

The phase comparator 20 as shown in Figure 6, is structured for example as has been displayed in Figure 7 and the comparison results obtained as a result of comparing the standard clock and it outputs either Up or Down signals.

**[0037]**

The charge pump that has been shown in Figure 6 is structured for example as has been displayed in Figure 8 and outputs the voltage signal on the basis of the UP signal and the Down signal from the phase comparator.

**[0038]**

The VCO 23 is constituted from the V-I converter (voltage current converter) 24, the IDAC 25 (current D/A converter) and the ICO 26 (current control oscillator).

**[0039]**

Further, PLL 18 is equipped with the control circuit 27 that controls IDAC 25. Based on the control signal from the control circuit 27, IDAC 25 changes the current signal from the V-I converter (voltage current converter) and then outputs the same. Then, ICO 26 output the frequency oscillation that corresponds to the current signal that has been changed and the oscillation frequency is hereby fluctuated. The V-I converter 24 is structured for example as has been displayed in Figure 9, and the voltage input  $V_i$  is converted into the current  $I_o$  and then outputted.

**[0040]**

ICO 26 is structured for example as has been displayed in Figure 10 and oscillates the clock with the frequency corresponding to the current input  $I_i$

**[0041]**

IDAC 25 is for example, structured as has been shown in Figure 11.

**[0042]**

IDAC 25 is the current D/A converter composed from  $n$  bits, and is also made up from the multiple current sources that comprise of current mirror circuits. Based on the input digital signals  $D_0, D_1, \dots, D_n$ , the current sources is cut off and an analog signal corresponding to the input digital signal is outputted

**[0043]**

The input digital signals  $D_0 \sim D_n$  are supplied to the NMOS transistor 36 1 36  $n$ .

The NMOS transistor 36 1 36  $n$  executes the switch operation and selects the current source that corresponds to the input digital signal. In other words, the current circuit (current mirror circuit which consists of any of NMOS transistors that exists within the NMOS transistor 35 1 35  $n$  and NMOS transistor 34) are selected. Then, current flows from the selected current mirror circuit and analog signals are outputted from the output terminal  $I_{out}$ .

**[0044]**

Based on the transistor size ratio ( $W/L$ ) such as the ratio of the channel width  $W$  to channel length  $L$  of the NMOS transistor 35 1 35  $n$ , the current mirror circuits are given the weight. The numbers  $2^n, 2, 4, \dots, 2^n$  which have been recorded on the upper portion of the NMOS transistor 35 1 35  $n$ , show the weight given.

**[0045]**

In IDAC 25, the front step portion that has been composed from PMOS transistor 29, 30 and 31 as well as NMOS transistor 32 and 33, determines the extent of the range to change the ICO oscillations frequency by keeping the frequency of the standard clock as the center. For example, when the frequency signal within the range of  $20\% + 20\%$  of the standard clock frequency is oscillated from the ICO, then, the size ratio of the PMOS transistor 29, 30 and 31 is set at a level of  $1:0.8:0.2$  and the transistor size ratio of the NMOS transistor 32 and 33 is set at a level of  $1:1$ . By making these settings, the frontal step portion of the IDAC 25, based on the current input, controls the ICO in such a manner that the standard clock frequency is oscillated at a frequency within the range of  $20\% + 20\%$ .

**[0046]**

Figure 12 shows the 1<sup>st</sup> example of the control signal that is outputted from the control circuit 27. The control signals that are outputted from the control circuit 27 are modulated waveforms as have been shown in Figure 12.

**[0047]**

Figure 13 shows the control circuit 37, which is the Example No. 1 of the control circuit 27.

**[0048]**

The control circuit 37 is a logic circuit that is a combination of the counter circuits. It has been composed from the up down counter 38 and the frequency divider counter 39. The Up Down counter 38 is based on the clock CLK and executes either increments or decrements. The frequency divider counter 39 divide the clock CLK into  $1/8$ , and in order to switch the Up Down counter 38's increment and decrement, outputs the Up down switch signal.

The Up Down counter 38, for example, when it has the Up Down switch signal as "1", increments the clock CLK's 8 counter part.

When the Up Down switch signal is "0" the clock CLK's 8 counter portion get decremented. As a result, the control signal becomes a modulated waveform as has been shown in Figure 14.

[0049]

Figure 15 shows the control circuit 40, which is Example No 2 of the control circuit 27.

[0050]

The control circuit 40 as has been shown in Figure 15 is composed from microcomputer 41. Based on the controls of microcomputer 41, it would be okay to output control signals as have been displayed in Figure 12 and Figure 14.

[0051]

Figure 16 shows the control circuit 42, which is Example No 3 of the control circuit 27.

[0052]

The control circuit 42 as has been shown in Figure 16 is constituted from register 43, microcomputer 44 and memory 45. On the basis of the controls of micro computer 44, the contents that have been stored in memory 45 are stored temporarily in the register 43 and it would be alright even if the contents that have been stored in register 43 are outputted as the control signals.

[0053]

Figure 17 shows the Example No. 3 of the control circuit that is outputted from the control circuit 27.

[0054]

Figure 18 is the frequency spectrum when modulation is done for the data from Figure 17 as control signals.

[0055]

Figure 19 is the frequency spectrum when modulations are done for the data from Figure 12 as control signals. As has been displayed in Figure 19, when the data from Figure 12 is used as control signals, there are cases sometime when a small peak in both the ends of the special frequency spectrum can be achieved. In such a case, the frequencies on both ends become the frequency with the maximum frequencies. However, with respect to the electronic devices and the system, since it is common that they are designed to operate by the frequencies of the central portion of the frequency spectrum, it is desirable to make the frequency with the maximum occurrence as the central part of the frequency spectrum.

As a result, the data that has been shown in Figure 7 is used as control signals. By making the slope of vicinity of the maximum values and the vicinity of minimum values steep, the frequency of occurrence of the frequencies on both ends is reduced. Further, by making the slope in the vicinity of control signals not steep, the frequency of occurrence of the frequencies in the middle portion is increased. By making use of the data that is shown in Figure 17 as the control signal, the frequency in the central part can be made to occur for a maximum number of times and it enables to obtain the frequency spectrum, which has been displayed in Figure 18.

**[0056]**

Apart from this, the control signals that are outputted from the control circuit 27 could also be randomly generated data.

**[0057]**

In such a manner, in the Working example 1 of the present invention, the current supplied to ICO 2 using IDAC 25 is made variable and subsequently the oscillation frequency of ICO 26 is made variable. As a result, the peak of the oscillation frequency spectrum that has been shown in Figure 4 is dispersed and the electromagnetic waves that are radiated from PLL are reduced.

**[0058]**

In working example 1 of the present invention, the oscillation frequency within a very short span of time becomes variable and the average wavelength that is oscillated from PLL is exactly the same as the traditional PLL and there is no problem.

**[Working Example 2 of the present invention]**

Figure 20 shows the Working example 2 of the present invention.

**[0059]**

Working example 2 of the present invention is a clock generator circuit, which simultaneously generates Clock Number 1 and clock No. 2, and by making the frequencies of one side of any clocks variable, it aims to reduce the electro magnetic radiation from clock generation circuits.

**[0060]**

For example, depending on the electronic devices, there are cases when some components or parts require precise clocks.

In such type of components, it is not possible to fluctuate even very slightly the frequencies of the clocks.

Working example 2 of the present invention is designed for electronic equipment that houses such components and ensures that the frequencies within many multiple clocks that may be generated are not fluctuated.

**[0061]**

The clock generator circuit 46 in working example 2 of the present invention is constituted from the Number 1 clock generator portion which is made from PLL 47 that outputs from the 1<sup>st</sup> operation clock CLK and, the Number 2 clock generator portion that outputs the 2<sup>nd</sup> clock CLK2 after receiving current signals from PLL 47.

**[0062]**

The PLL 47 that composes the 1<sup>st</sup> clock generator portion is actually constituted from 1/N frequency divider 48, phase comparator 49, charge pump 50, loop filter 51, VCO (voltage control oscillator) 52 and 1/M frequency divider 55 and apart from the configuration of VCO, it is the same as PLL 18 that has been shown in the working example 1 of the present invention that has been displayed in Figure 6.

**[0063]**

VCO 52 is composed from the V-I converter 53 and the 1<sup>st</sup> ICO (current control oscillator) 54.

**[0064]**

The V-I converter 53 converts the voltage signal that is supplied from the loop filter 51 into the current signal and the 1<sup>st</sup> ICO54 outputs 1<sup>st</sup> clock CLK 1 of the frequency that is corresponding to the current signal.

**[0065]**

IDAC 57 which makes up the 2<sup>nd</sup> clock generator part change the current signal that is outputted from the VCO 52's V-I converter 53 on the basis of the control signals from control circuit 56 and outputs it. The 2<sup>nd</sup> ICO 49 outputs the 2<sup>nd</sup> clock CLK 2 of the frequency that corresponds to the modified current signal, then, the oscillation frequency is changed. However, control circuit 56 is equipped with the same configuration as the control circuit shown in Figures 13, 15 and 16, but at the same time, it is not limited to this type of a configuration alone.

**[0066]**

As the frequency of the 1<sup>st</sup> clock CLK 1 that is generated in the 1<sup>st</sup> clock generator portion cannot be made variable, it is also not possible to reduce the electromagnetic radiation. However, the frequency of the 2<sup>nd</sup> clock CLK 2 that is generated in the 2<sup>nd</sup> clock generator portion can be made variable by supplying variable current signal to the 2<sup>nd</sup> ICO58 from IDAC 57. Consequently, the clock generator circuit in the current invention's working example 2 can reduce the electromagnetic radiation.

**[Working Example 3 of the current invention]**

Figure 21 shows the Working example No. 3 of the current invention.

**[0067]**

Working example 3 of the present invention is equipped with almost the same configuration as has been shown in working example 2 in Figure 20. The points where it differs from working example 2 is the point where the supplementary IDAC 67 within the VCO of the PLL that constitutes the 1<sup>st</sup> clock generator portion is set up.

**[0068]**

We shall now consider the case when the IDAC 72 did not change the current signals from the V-I converter 66.

The 1<sup>st</sup> ICO68 that supplies the same current signals from the V-I converter 66 and the 2<sup>nd</sup> ICO 73 should actually output the clock with the same frequency. However, due to the dispersion in manufacturing processes, there are cases of differences in the clocks.

**[0069]**

Because of that, the IDAC 66 that is used to correct the current signal from the V-I converter 66 is inserted in between V-I converter 66 and the 1<sup>st</sup> ICO 68. The corrective IDAC 67 is controlled by control circuit (2) 68, the current signal  $I_c$  wherein the error caused by manufacturing inconsistency is corrected is supplied to the 1<sup>st</sup> ICO67. On account of the correction of this error, the PLL 60, which composes the 1st clock generator part, can also generate the 1<sup>st</sup> clock CLK1 and it hence enables to realize a high precision clock generator circuit. The configuration of the control circuit (2) which controls the corrective IDAC 67 is also used for the purpose of adjustments and could be terminal clips such as GND clips and current power clips. Or it can be composed of register.

**[0070]**

However, in working example No. 3 of the present inventions, similar to working example No. 2 of the invention, the frequency of the 2nd clock CLK2 which is generated by the 2<sup>nd</sup> generator portion can be made variable based on the supply of the variable current signal to the 2<sup>nd</sup> ICO 73 by IDAC 72. Consequently, the clock generator circuit in the present invention's working example 3 can most conclusively and definitely reduce the radiation of the electromagnetic waves

**[Working Example 4 of the present invention]**

Figure 22 shows the working example 4 of the present invention.

**[0071]**

Working Example 4 is equipped with almost the same structure as Working Example 1 of this invention as shown in Figure 6. The point of difference with Working Example 1 is the use of IDAC 79 attached to the LPF (low pass filter) as the IDAC.

**[0072]**

Figure 23 shows an example of the IDAC with the attached LPF.

**[0073]**

The IDAC with the attached LPF as shown in Figure 23 possesses almost the same configuration as the IDAC shown in Figure 11 but is still different from the IDAC in Figure 11 and is equipped with LPF which is constituted from PMOS transistor 93 and 96 in the current output part, resistance 94, condenser 95 and NMOS transistor 97 and 98

**[0074]**

In the IDAC, there are cases when glitch (noise) occurs in the current output at the time of changing the input data. If this glitch is sent to the ICO, the ICO output a high frequency signal corresponding to the glitch. As a result, PLL move out of the locked state and could possibly come to a stage when it could not be maintained in the standard frequency.

**[0075]**

Hence, if an IDAC with an LPF is made use of in order to smoothen out the current output, it enables to smoothen out the current output that generated the glitch and PLL not longer moves out of the locked state. It enables to provide a PLL that has a high level of accuracy.

**[0076]**

Related to the explanation given above, the following is also explained.

**(Additional Note 1)**

Regarding the clock generator circuit equipped with the phase comparator which is inputted by a standard clock and operating clock and a voltage control oscillator that generated the aforementioned operating clock based on the output signal of the aforementioned phase comparator, the clock generator circuit has the characteristics wherein the aforementioned voltage control oscillator comprises of a voltage current converter that converts the voltage signal into an current signal, an variable current circuit which can fluctuate the aforementioned current signal and an current control oscillator that oscillates the frequencies based on the aforementioned variable current signals. (Claim 1)

**(Additional Note 2)**

A clock generator circuit as mentioned in Claim 1 that is characterized by the presence of the aforementioned variable current circuit, which could be a current D/A converter or a current D/A converter with an attached Low pass filter (Claim 2)

**(Additional Note 3)**

A clock generator circuit as has been mentioned in the Additional Note 1, which is characterized by the presence of a control circuit that controls the aforementioned variable current circuit.

**(Additional Note 4)**

The characteristics of the clock generation circuit described in the additional note 1 is that the aforementioned current variable circuit is equipped with the means to determine the range of change of frequency of clock which is oscillated by the aforementioned current control oscillator.

**(Additional Note 5)**

It is a clock generator circuit wherein the results of comparison between the standard clock the comparison clock are converted to current signals and based on the aforementioned current signals, the operation clock is generated, and furthermore, the characteristics of the aforementioned clock generator circuit is equipped with Circuit No 1 that generate multiple current signals by changing the aforementioned current signal and Circuit No 2 which generates clocks with multiple varying frequencies based on the aforementioned multiple current signals.

(Claim 3)

**(Additional Note 6)**

The characteristics of a clock generator circuit as has been mentioned in the Additional Note 5 that the aforementioned 1<sup>st</sup> circuit is the current D/A converter or a current D/A converter attached with a low pass filter.

**(Additional Note 7)**

A clock generator circuit as has been mentioned in the Additional Note 5, which is equipped with a control circuit that controls the aforementioned 1<sup>st</sup> circuit.

**(Additional Note 8)**

A clock generator that is characterized by the presence of a phase comparator which outputs The results of comparison between the standard clock and the comparison clock, and Circuit No 1 that generates current signals based on the results of the aforementioned comparison as well as Circuit No. 2 that Generates current Signal No. 1 and Current signal No. 2 based on the aforementioned current signal. Further the clock generator circuit also is equipped with a 3<sup>rd</sup> circuit that generates a 2<sup>nd</sup> frequency clock based on the aforementioned 2<sup>nd</sup> current signal along with the generation of the clock with the first frequency based on the aforementioned 1<sup>st</sup> Current signal.

(Claim 4)



**(Additional Note 9)**

The characteristics of the clock generator circuit as has been mentioned in the Additional Note 8 is that the aforementioned 1<sup>st</sup> circuit is the current D/A converter or a current D/A converter attached with a low pass filter.

**(Additional Note 10)**

A clock generator circuit as has been mentioned in the Additional Note 8 that is equipped with a control circuit that controls the aforementioned 1<sup>st</sup> circuit.

**(Additional Note 11)**

Regarding the clock generator circuit which is equipped with the 1<sup>st</sup> clock generator part that generates the 1<sup>st</sup> clock, and the 2<sup>nd</sup> clock generator part that generates the 2<sup>nd</sup> clock, wherein the 1<sup>st</sup> clock generator part is equipped with the phase comparator which compares the standard clock and the operating clock and a voltage current converter that converts the signal based on the aforementioned comparison results or the comparison results into current signals as well as the as the 1<sup>st</sup> voltage control oscillator that generated the 1<sup>st</sup> operating clock based on the aforementioned current signal. Further the 2<sup>nd</sup> clock generator part comprises of the variable current circuit that can convert the aforementioned current signals and the 2<sup>nd</sup> current control oscillator that oscillates the frequency clock based on the aforementioned variable current signal. (Claim 5)

**(Additional Note 12)**

A clock generator circuit as has been mentioned in the Additional Note 11, wherein the aforementioned current variable circuit is a current D/A converter or a current D/A converter attached with a low pass filter.

**(Additional Note 13)**

A clock generator circuit as has been mentioned in the Additional Note 11 wherein there is a control circuit that controls the aforementioned current variable current circuit.

**(Additional Note 14)**

The characteristics of the clock generation circuit described in the additional note 11 is that the aforementioned current variable circuit is equipped with the means to determine the range of change of frequency of clock which is oscillated by the aforementioned 2<sup>nd</sup> current control oscillator.

**(Additional Note 15)**

The characteristic of the clock generator circuit as has been mentioned in the Additional Note 11 is that the aforementioned 1<sup>st</sup> clock generator part is equipped with the corrective circuit which corrects the aforementioned current and supplies the same to the aforementioned 1<sup>st</sup> voltage control oscillator.

**(Additional Note 16)**

Regarding the clock generator circuit that generated a 1<sup>st</sup> clock of a frequency spectrum containing N number of peaks (N is an integer that is greater than 1A), the clock generator circuit is characterized by the presence of the methods as follow: on the basis of the current signal which is generated by the comparison results obtained between the standard clock and the

comparison clock, it is equipped with a method to generate the 2<sup>nd</sup> clock containing a frequency spectrum with M number of peaks (N is an integer that is greater than 1,  $M > N$ ).

(Claim 6)

**(Additional Note 17)**

The characteristics of the clock generator circuit as has been mentioned in the Additional Note 16 is that the aforementioned method includes a current D/A converter or a current D/A converter that is attached to a low pass filter which changes the aforementioned current signal.

**(Additional Note 18)**

Regarding PLL that is equipped with a phase comparator that inputs a standard clock and an operating clock and, a charge pump that supplies the output of the aforementioned charge pump, and a voltage control oscillator that outputs the aforementioned operating clock along with the supply of output of the aforementioned charge pump, the characteristics of PLL is that the above mentioned voltage control oscillator is equipped with a voltage current converter that converts the voltage signal into the current signal, an current variable current circuit that can change the aforementioned current signal and a current control oscillator that oscillates the frequency based on the aforementioned variable current signal.

(Claim 7)

**(Additional Note 19)**

Regarding the operation clock generation method, the characteristics of operation clock generation method is that the standard clock and the comparison clock are compared and the results of the aforementioned comparison is converted into current signals, the aforementioned current signals are changed based on the control signal, and the operating clock with varying frequencies is outputted based on the above mentioned variable current signal.

(Claim 8)

**(Additional Note 20)**

A operation clock generation mechanism is characterized by comparing the standard clock and the comparison clock, converting the results of the aforementioned comparison into current signals, generating the 1<sup>st</sup> current signal and the 2<sup>nd</sup> current signal basing the above mentioned current signal on the control signal, and then generating the 1<sup>st</sup> frequency clock based on the aforementioned 1<sup>st</sup> current signal and also generating the 2<sup>nd</sup> frequency clock based on the aforementioned 2<sup>nd</sup> current signal. (Claim 9)

**(Additional Note 21)**

A clock generator circuit is characterized by comparing the standard clock and the comparison clock, and generating multiple current signals on the basis of the aforementioned results of comparison and further generating a clock with frequency spectrum containing M number of peaks (M is an integer that is greater than 2) based on the aforementioned current signals.

(Claim 10)

[0077]

**[Effects of the invention]**

Based on the current invention, it enables to achieve the following results.

- (1) The oscillation frequency spectrum can be effectively diffused and the electro magnetic radiation can be reduced.
- (2) It is possible to freely set the degree of diffusion of the oscillation frequency spectrum.

- (3) It is possible to accurately transition the oscillation frequency spectrum.
- (4) It is also possible to effectively deal with the dispersion on account of process fluctuation, temperature fluctuation and fluctuations in the power source voltage etc.
- As this invention is able to achieve the above, it becomes particularly useful in electronic devices where it is necessary to control the electromagnetic radiation such as in printers.

**[A brief explanation of the diagrams]**

**[Diagram 1]**

This figure shows the traditionally used PLL.

**[Diagram 2]**

This is a graph showing the frequency spectrum of the traditionally used PLL.

**[Diagram 3]**

This is a logical representation of the present invention

**[Diagram 4]**

This is a graph showing the frequency spectrum-1 of the clock generator circuit.

**[Diagram 5]**

This is a graph showing the frequency spectrum-2 of the clock generator circuit.

**[Diagram 6]**

A diagram showing the Working Example 1 of the invention.

**[Diagram 7]**

This is a diagram showing an example of the phase comparator

**[Diagram 8]**

This is a diagram showing an example of the charge pump.

**[Diagram 9]**

This is a diagram showing an example of the V-I converter

**[Diagram 10]**

This is a diagram showing an example of the ICO.

**[Diagram 11]**

This is a diagram showing an example of the IDAC

**[Diagram 12]**

This is a diagram showing the 1st example of the control signals

**[Diagram 13]**

This is a diagram showing the first example of the control circuit that controls the IDAC.

**[Diagram 14]**

This is a diagram showing the 2<sup>nd</sup> example of the control signals

**[Diagram 15]**

This is a diagram showing the second example of the control circuit that controls the IDAC.

**[Diagram 16]**

This is a diagram showing the third example of the control circuit that controls the IDAC.

**[Diagram 17]**

This is a diagram showing the 3rd example of the control signals

**[Diagram 18]**

This is a graph showing the frequency spectrum-3 of the clock generator circuit.

**[Diagram 19]**

This is a graph showing the frequency spectrum-4 of the clock generator circuit.

**[Diagram 20]**

This is a diagram showing the Working Example 2 of the invention.

**[Diagram 21]**

This is a diagram showing the Working Example 3 of the invention.

**[Diagram 22]**

This is a diagram showing the Working Example 4 of the invention.

**[Diagram 23]**

This is a diagram showing an Example of the IDAC with the LPF.

**[Explanation of the symbols]**

1/N frequency divider

Phase comparator

Charge pump

Loop filter

VCO

1/M frequency divider

V-I converter

IDAC

IDAC with LPF

ICO

Control circuit

Refer to the traditional

**[Document name]   Abstract**

**[Abstract]**

**[Subject]**

It aims to provide a clock generator circuit wherein the oscillation frequency spectrum is diffused and the electro magnetic radiation can be reduced.

**[Means to solve the problems]**

The results obtained by comparing the standard clock and the comparison clock are converted into current signals and, based on the relevant current signals and by changing the oscillation frequency, the oscillation frequency spectrum of the clock generator circuit can be dispersed and a reduction in the electromagnetic radiation can be achieved.

**[Selected diagrams]   Diagram 3**

[Document Name] Diagram

**[Diagram 1]**

The traditionally used PLL

3 Phase comparator

**[Diagram 2]**

Frequency spectrum of the traditionally used PLL

**[Diagram 3]**

Logical representation of the present invention

10 Phase comparator

V-I converter

Current variable circuit

**[Diagram 4]**

Frequency Spectrum-1 of the present invention's clock generator circuit

**[Diagram 5]**

Frequency Spectrum -2 of the present invention's clock generator circuit

**[Diagram 6]**

Working example 1 of the current invention

20 Phase comparator

V-I converter

27 Control circuit

**[Diagram 7]**

An example of the phase comparator

Standard clock

Up signal

Comparison clock

Down signal

**[Diagram 8]**

An example of the charge pump

Up signal

Down signal

Current signal

**[Diagram 9]**

An example of the V-I converter

Voltage  $V_i$

Current  $I_o$

**[Diagram 10]**

An example of the ICO

Current  $I_i$

**[Diagram 11]**

An example of the IDAC

Size ratio

**[Diagram 12]**

Example No. 1 of the control signal

Y-axis: Control signal

X-axis: Time  $t$

**[Diagram 13]**

Example No. 1 of the control circuit

38 Up Down counter - Control signal

39 frequency Divider counter      Up down switching signal

CLK

Up down switching signal

**[Diagram 14]**

Example No. 2 of the control signal

Y-axis: Control signal

X-axis: Time  $t$

**[Diagram 15]**

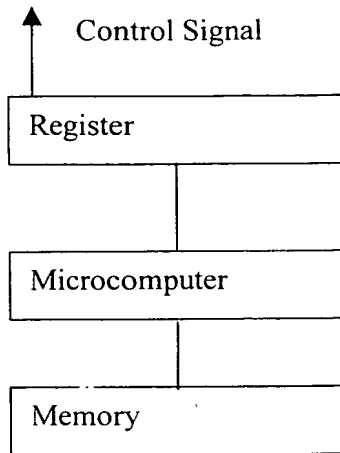
Example No. 2 of the control circuit

↑ Control signal

Micro computer

**[Diagram 16]**

Example No. 3 of the control circuit



**[Diagram 17]**

Example No. 3 of the control signal

**[Diagram 18]**

Frequency Spectrum-3 of the present invention's clock generator circuit

**[Diagram 19]**

Frequency Spectrum - 4 of the present invention's clock generator circuit

**[Diagram 20]**

Working Example 2 of the present invention

49 Phase comparator

V-I converter

56 Control circuit

**[Diagram 21]**

Working Example 3 of the present invention

62 Phase comparator

V-I converter

67 IDAC used for correction

70 Control circuits 2

71 Control circuit 1

**[Diagram 22]**

76 Phase comparator

V-I converter

84 Control circuit



**[Diagram 23]**

Example of an IDAC with LPF

Tr Size ratio